Analog boost switching power supply study

Part 1. Draft

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Circuit description The circuit is the control inductor L_2 which is being switched from $V_{out} - V_{in}$ to $-V_{in}$ delta V by FET M2 with some duty; Diode D_2 and the output stage (which would show up as plant in the linear analysis) with a buffering capacitor C_4 and test resistive load R_{load} along with a load disturbance voltage controlled biased FET M3 and R_5 as bias.

M_2 is biased essentially to ground, so that $\frac{L_2}{R_{channel}+R_{15}}$ is very long: about 10 seconds. The gate is RC filtered by R_4 and C_5 to prevent high (capacitive?) current overshoots during turn-on.

The clock in the circuit is the 2-bjt flip-flop (Q_1, Q_2). The duty is controlled by R_3 and C_2 and by C_1 and a voltage controlled resistance via FET M_1 and bias $R_7 = R_3$.

The feedback tied, error based, control signal is fed to the gate of M_1. For simplest control scheme attempted so far, the gate drive would be two comparators, one op-amp and one divide. Instead of the electronics for spice simulations a synthetic voltage controlled voltage source B_1 is programmed as:

$$V = \min(\max(0., K\frac{V_{out} - V_{ref}}{V_{out}}), 5) + 3.4 \tag{1}$$

Biasing details

The biased FET M2 is a voltage controlled resistor. The 500 Ohm line intersects saturation region flat lines which are spaced evenly in gate voltage which is defined with respect to ground (not drain). The curren in mA is:

$$I = 3.2 + 2.1 \times (V_{ctrl} - 4) \tag{2}$$

The actual resistance of the duty controlling arm R_1 is set by voltage difference between V_{cc} and the gate of Q1 with average of roughly half of $-V_{cc}$. When Q1 turns off, Q2 turns on, and the voltage difference across C1 is not changed (fixed charge transient). So, this means that the gate of Q2 gets pulled down by as much as V_{cc} down keeping it off until C1 equilibriates via R1. In practive, we take the voltage difference as αV_{cc}, $\alpha > 1$, so:

$$R_1 = \frac{\alpha V_c c}{I} \tag{3}$$

The ratio of duties of the two sides is the ratio of the resistances:

$$\frac{d}{1-d} = \frac{R_1}{R} = \frac{1000}{500} \frac{\alpha V_{cc}}{3.2 + 2.1(V_{ctrl} - 4)} \approx \frac{\alpha V_{cc}}{V_{ctrl} - 2.5} \tag{4}$$

So,

$$d = \frac{\alpha V_{cc}}{V_{ctrl} - 2.5 + \alpha V_{cc}} \tag{5}$$

$$1 - d = \frac{V_{ctrl} - 2.5}{V_{ctrl} - 2.5 + \alpha V_{cc}} \tag{6}$$

With the chosen V_{cc} of 15 V, that term dominates in the denominator, so approximately:

$$1 - d \approx 0.03(V_{ctrl} - 2.5) \tag{7}$$

Basic linearization The output side of the inductor has a pwm averaged voltage of $(1 - d)V_{out}$ with d the ON duty of M2. This means that the control signal comes in via the coefficient of the equations and if made simply proportional to $V_{ref} - V_{out}$ these equations become non-linear. To overcome this, the error is defined differently, normalizing it by the output voltage:

$$e \equiv \frac{V_{out} - V_{ref}}{V_{out}} \tag{8}$$

$$1 - d \equiv \min(0.1, \max(0.0, K \times e)) \tag{9}$$

The setting of duty complement to V_{out} scaled error in practice means, that the control voltage at the gate of M2 is:

$$1 - d \approx 0.03(V_{ctrl} - 2.5) = \min(0.1, \max(0.0, K \times e)) \quad (10)$$

$$V_{ctrl} \approx 2.5 + \min(3, \max(0.0, K \times e)) \quad (11)$$

Notice that this forces the error to be positive wrpt reference voltage. This makes the control unstable when the power supply turns on, meaning duty hits the allowed ceiling and stays there until voltage overshoots V_{out} at which point linear control kicks in. When the error is sufficiently small, the equations for the plant and the controller reduce to in open loop:

$$\begin{aligned} V_{in} - L\dot{I}_L &= (1-d)V_{out} \\ C\dot{V}_{out} + \frac{V_0}{R} &= I_L \\ V_{out} &= \frac{V_{in}}{1-d}\frac{1-d}{LCs^2 + \frac{L}{R}s + (1-d)} \end{aligned}$$

and in closed loop with this choice of error:

$$\begin{aligned} 1 - d &\equiv K \times e \\ V_{out} &= V_{ref}\frac{\frac{V_{in}}{V_{ref}} + K}{LCs^2 + \frac{L}{R}s + K} \end{aligned}$$

Performance: open and closed loop Assessment of linearity, load independence of output voltage and control duty and feed forward table numbers. $V_{in} = 5, L = 1mH, C = 30mF, R_{load} = 70\Omega, R_{loaddist} = 5\Omega$. P only controller test points with $K = 10000$

1 The circuit does not entirely behave as per linear analysis in open-loop. The achieved output voltages are higher then the $\frac{V_{in}}{1-d}$ calculation with duty directly extracted from the control FET gate as $\frac{<V_{ctrl}>}{V_{cc}}$

2 Another deviation from the linear analysis is some dependence on the output load of the steady state output voltage (linear analysis says there is none in open loop even). One place where this is clearly understandable is when the control inductor goes into discontinous

Table 1: Circuit performance sweep to 50 V output: open and closed loop

V_{in}	V_{ctrl}	$V_{clock,ave}$	d	$\frac{V_{in}}{1-d}$	V_{out}	ΔV_{out}	ΔV_{out} w ctrl	ΔP	P
5	8.	9.75	0.65	14.3	14.5	na	na	na	na
5	5.0	11.8	0.74	23.1	23.8	na	na	na	na
5	4.5	12.2	0.81	26.8	29.2	3.	0.3	4.9	12.
5	3.85	12.8	0.85	33	40.	1.	0.4	5	23
5	3.5	13.2	0.88	41.5	48.	1.2	1.5	5	33

conduction mode (at low loads the current can drop to 0 and then the simple linear analysis no longer applies ... and the output voltage would depend on the duration of the 0 current interval which can be load dependent)

3 With feedback and P-only, high gain control running, the error on the reference is worse when the controller saturates and starts acting as a poor bang-bang controller. Even in that case in mid-range of output voltage ($\frac{V_{out}}{V_{in}} = 6$) the error swing due to load variations is 10 times smaller than in open loop. When the controller does not saturate, the tracking error is very small, on the order of 0.1%. Empirically, high gain does not appear a problem as the min/max saturation blocks act as stabilizers at high error

Controller design via linear analysis and next steps Some observations about open loop operation are:

1 Imperfect linearity and a need to for a look up feedforward table with some load dependence

2 Response rate and damping is strongly dependent on the load

The second point would persist even with the P-only controller and requires compensation to mitigate. In time domain we now scale the controller output by output voltage and maintain the error in the standard form as $V_{out} - V_{ref}$:

$$
\begin{aligned}
1 - d &\equiv \frac{1}{V_{out}} D(e) && (12)\\
e &\equiv V_{out} - V_{ref} && (13)\\
V_{in} + DV_{ref} &= (LCs^2 + \frac{L}{R}s + D)V_{out} && (14)\\
G &\equiv \frac{1}{LCs(s + \frac{1}{RC})} && (15)\\
V_{out} &= \frac{DG}{1 + DG} V_{ref} + \frac{G}{1 + DG} V_{in} && (16)
\end{aligned}
$$

The plant has a pole at the origin and another at $\frac{1}{RC}$. We want to move the closed loop polynomial poles ($1 + DG$) to the left so that the damping is not dependent on R, or weakly dependent. We chose the compensation as a lead compensator with a gain. So,

$$D = K \frac{p}{z} \frac{s + z}{s + p} \tag{17}$$

α value is at $\approx \frac{p-z}{2}$ as the plant poles are near the origin over a range of R values. A sequence of root loci for R swept from 0.1 to 1000 Ohms is plotted with a $p = 10000, z = 2500$. A gain of about 400 would give damping of 0.5 and overshoot of 16 % essentially independently of the load

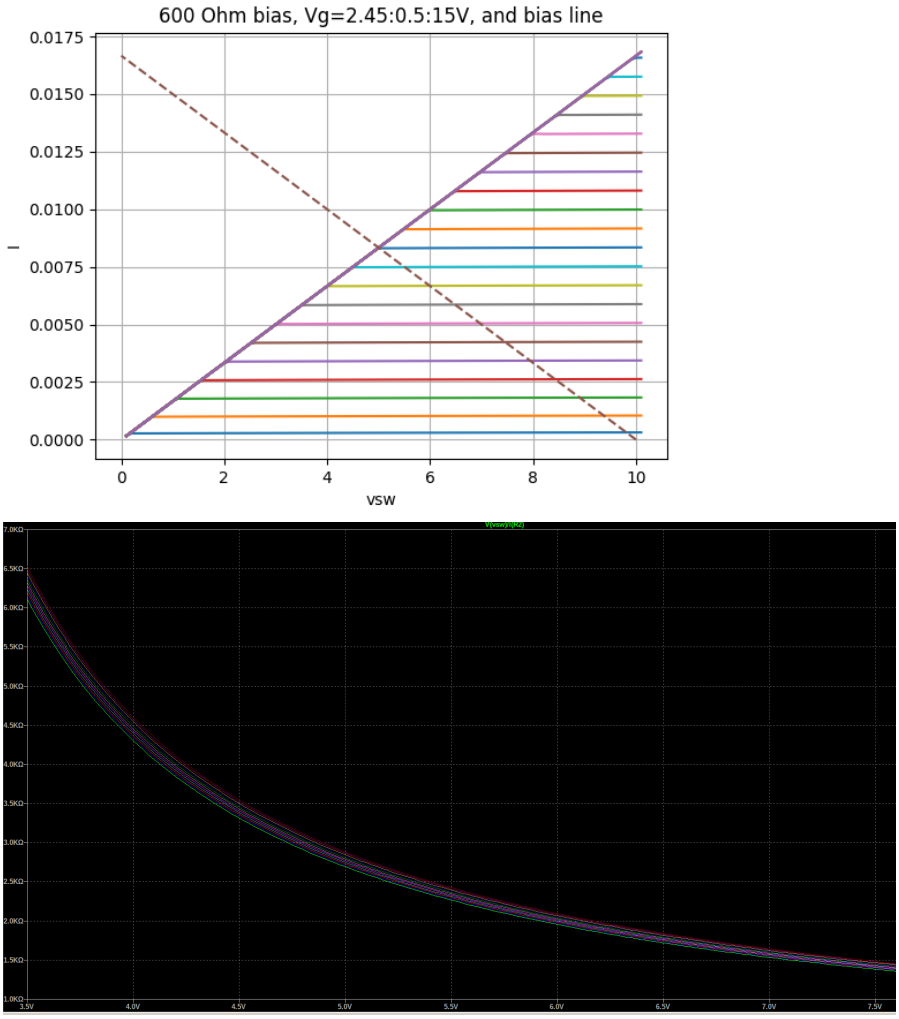

Figure 1: $M2$ biasing and variable resistance with gate-to-ground voltage

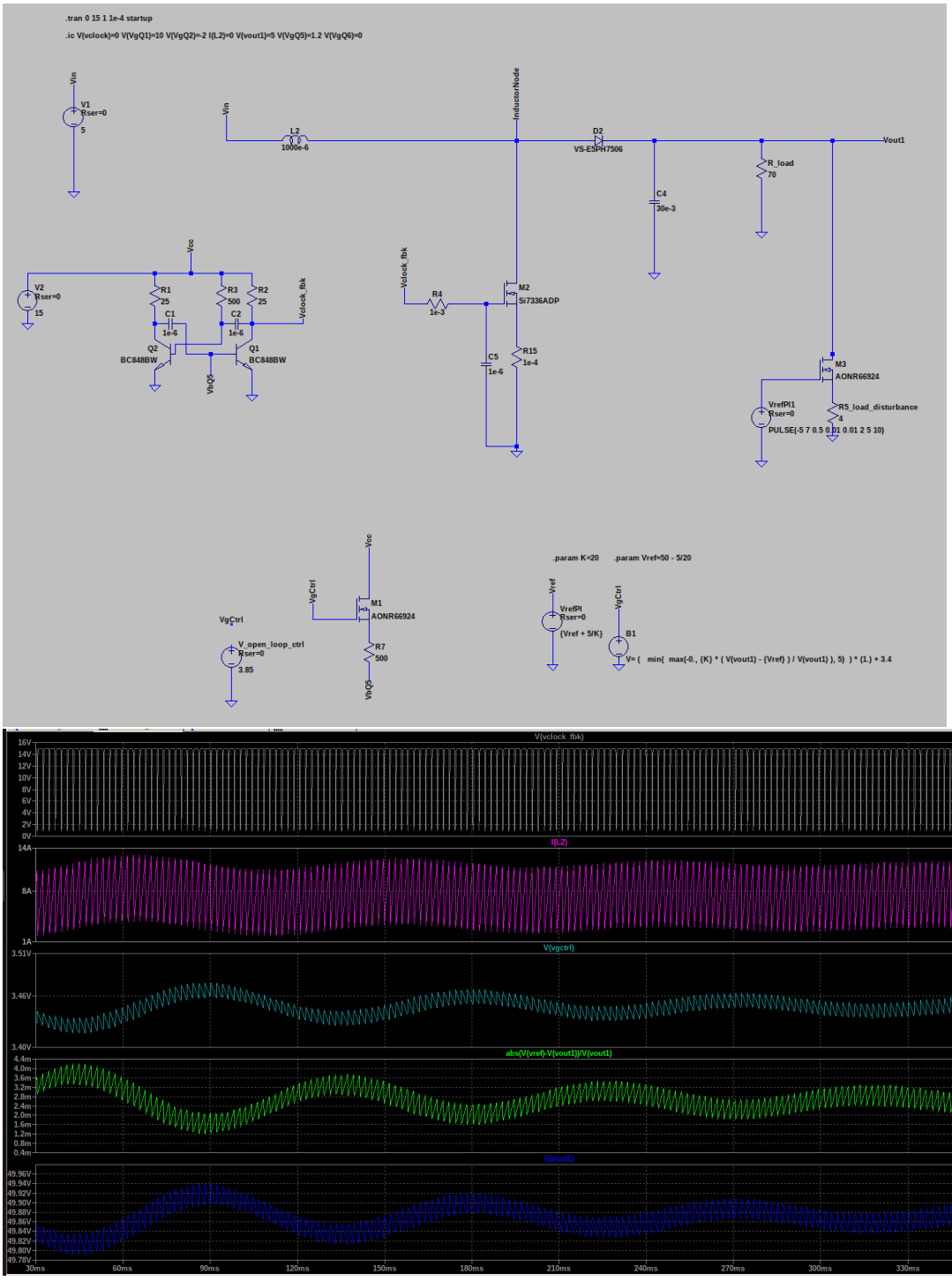

Figure 2: Example at $K = 20$ and $V_{out} = 50$ with controller running

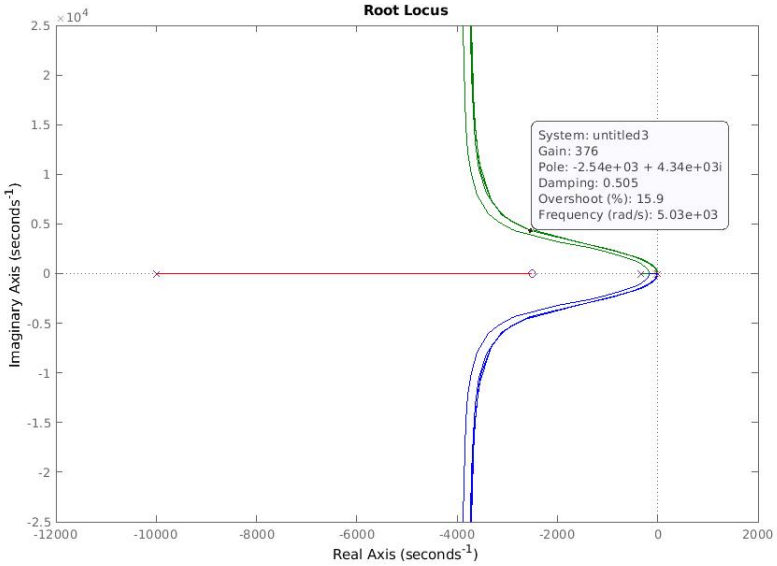

Figure 3: Root locus and gain choice for lead compensation over a range of R values

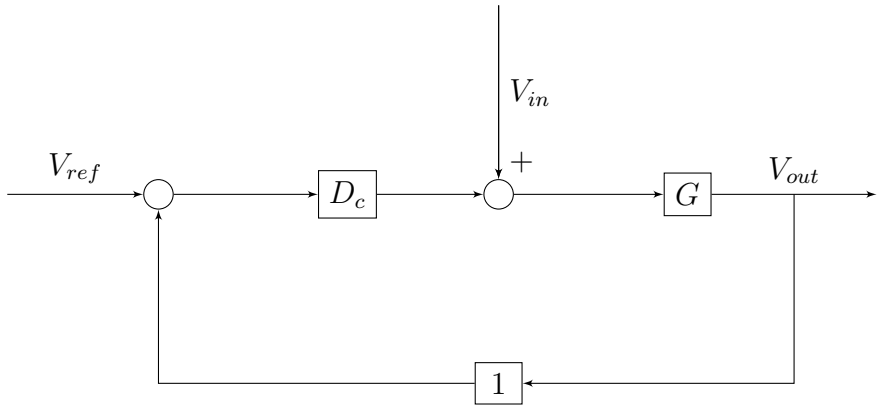

Figure 4: Control loop layout after linearization of feedback